Body-Biased VCO Tunes 12 To 16 GHz

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Abstract: This body-biased voltage-controlled oscillator provides reasonably good phase-noise performance over a broad tuning range with relatively low power consumption and low jitter timing noise in the time domain.

Voltage-controlled oscillators (VCOs) are an integral part of frequency synthesizers using phase-locked loops (PLLs) and clock and data recovery (CDR) circuits.[1] Phase noise is one of the most critical characteristics of the wireless communication systems and it is based on static behavior in the device oscillation.[2] In wireless communication systems, wide bandwidths with reliable phase noise performance is extremely critical; hence the phase noise performance has been improved by number of novel VCO structures.[1-6]

In this article, a novel dynamic-threshold (D_T) metal-oxide-semiconductor (MOS) (DTMOS) technique has been applied to increase the operating bandwidth of a VCO by reducing the threshold voltage (V_T) of a PMOS load transistor to achieve faster transitions and higher operating frequencies. The three-stage VCO has a center frequency of 14 GHz with tuning range of 12 to 16 GHz and phase noise of -101 dBc/Hz offset 100 kHz from the carrier.

In this novel VCO design, the reduction of threshold voltage V_T results in an exponential increase in the static power. This is a drawback in silicon-based technologies,[3] but having dynamic control over V_T can be a benefit in some oscillator designs. It helps overcome supply variations and noise injection,[4] and eliminate parasitic capacitors in the transistor (gate-source, gate-base, and gate-drain capacitances CGS, CGB, and CGD, respectively)—and device body effects when the PMOS transistor is turned off. This control can lead to broadband VCO tuning. The DTMOS approach works best with a low voltage supply; as a result, it is ideal for high-frequency applications requiring a low-voltage supply.

In a traditional VCO design (**Fig. 1**), a PMOS device is employed as resistor. Gate-source voltage V_{GS} is used to steer the frequency oscillation of the VCO. However, by changing V_{GS}, threshold voltage V_T varies dramatically, resulting in significant change in $V_{GS} - V_{TH}$, resulting in the PMOS device not functioning as a resistor and the VCO circuit failing to oscillate.

To maintain a PMOS device in the Ohmic region, the relation $V_{DS} < V_{GS} - V_T$ must be valid. As long as VGS steers the frequency, V_G cannot be changed over a wide-enough range for truly wideband tuning. Altering V_G causes the PMOS device to operate in the saturation region, leading to a failure to oscillate.[6]

Figure 2 shows the body-biased delay-cell topology for the proposed broadband VCO. This method guarantees that V_{GS} is always equal to V_{DD} hence the PMOS operating region will never go into saturation. By employing this bulk connection to the voltage control, there is a need to consider the influence of the source-to-body voltage, on threshold voltage V_T:

$$V_{TH} = V_{TH0} + \Gamma(V_{SB} + |2f_f|)0.5 - (|2f_f|)^{0.5} \quad (1)$$

where

V_{TH0} = zero-bias threshold voltage, f_f = the Fermi potential, V_{SB} = the source-to-body voltage, and Γ = the body effect coefficient.

The values of the minimum threshold voltage, V_{tmin}, and the maximum threshold voltage, V_{tmax}, based on variations in V_{SB} are shown in Fig. 3. Higher amplitudes of cause wider depletion regions for longer durations. This results in a wider voltage control range. Equation 1 impacts two cases: when V_B is at a minimum and when V_B is at a maximum.

In the first case, when $V_B = 0$, the relationship of V_{SB} with threshold voltage V_T is significantly small, but not negligible. This relationship provides a wide tuning range of V_B for steering the control voltage. When the bias voltage is zero, V_{SB} is equal to VDD. Hence,

$V_{TH} = V_{TH0} + 0.7$ V. Threshold voltage V_T is at a maximum value, resulting in a slow transition. This represents the worst-case scenario for the PMOS device to operate in the linear region, and leads to a lower-frequency tuning range for the VCO.

In the second case, when $V_B = 4$ V, and the control voltage is at its maximum, VSB is equal to zero, and, in Eq. 1, $V_{TH} = V_{TH0}$. This gives the minimum for V_T, which leads to a faster PMOS transition, and upper-frequency range for the VCO circuit.

Figure 3 shows behaviors for V_{tmin} and V_{tmax}. The second case is similar to the operation of a traditional VCO, in which the zero control voltage is biased to the gate connection to achieve higher-frequency operation. In this second case, when $V_B = 4$ V, the high voltage biasing configuration cannot be applicable unless using a thickgate PMOS transistor. Normally, thin-gate PMOS transistors cannot take more than 1.5 V because the electrical overstress (EOS) voltage will damage the device and ultimately lead to device breakdown.

For semiconductors, EOS presents a range of electrical threats due to electromagnetic pulse (EMP) and electrostatic discharge (ESD) effects. Device failure is the result of overloading the gate connection with too high a voltage. But in the proposed VCO design, the gate connection is grounded, allowing an increase in the bulk voltage, V_B; the rate at which positive charges in the depletion region discharge through the gate connection to ground increases as a result of this configuration. The higher amplitude of V_B causes a wider depletion region to last for a longer time over a wider control voltage range.

Figure 4 shows an MOS small-signal equivalent circuit for modeling high-frequency operation. Setting VG to zero eliminates the parasitic effects of C_{GS}, C_{GD}, and C_{GB} and also increases V_{GS}, which leads to an incremental increase in current source $g_m V_{GS}$. Biasing the device body to a voltage greater than zero results in decreases of C_{BD}, C_{BS}, and a decrease in V_{SB}, which decreases the leakage current of $g_{mb} V_{BS}$. Each VCO delay cell has a capacitance value of C_{total} which can be calculated by Eq. 2. By substituting C_{total} into Eq. 3, the VCO frequency can be calculated:

$$C_{total} = C_{GS} \text{ (in CMOS)} + {}_{CGB} \text{ (in PMOS)} + C_{DB} \text{ (in PMOS)} \quad (2)$$

$$F_{center} = 1/(2nRC_{total}) \quad (3)$$

In Eq. 2, the decrease of CGB (in PMOS) and C_{DB} (in PMOS) results in an increment of the upper frequency limit, leading to a more wideband VCO.

By biasing the bulk connection to a voltage greater than zero (Fig. 5), more electrons are attracted to the device substrate connection, leaving a larger positive charge. Therefore, the depletion region becomes wider. In Eq. 4, V_T is proportional to total charge in the depletion region because the gate charge must mirror Q_d before the inversion layer is formed[6,7]:

$$V_{TH} = f_{ms} + 2f_f + (Q_{dep}/C_{ox}) \quad (4)$$where f_{ms} is the difference between the work function of the polysilicon gate and the silicon gate, and

$$f_f = (KT/q) \ln(N_{sub}/N_i) \quad (5)$$

$$Q_{dep} = (4qe \, Sif_f V_{sub})^{0.5} \quad (6)$$

Note that the gate voltage is always zero. This configuration results in 1) discharging the large positive charge load in the depletion region due to positive body biasing, 2) fast forming in the channel between the drain and source connections, and 3) fast discharging of the charge load though the gate connection into ground, which finally leads to a much faster transition in an MOS device. Figure 6 shows the three-stage ring VCO, while Fig. 7 provides the simulated output spectrum for the VCO. The Table compares wideband VCOs.[8-12] The DTMOS methods shown here can be applied to achieve wideband VCOs capable of handling more than one communication channel, such as the example from 12 to 16 GHz with low phase noise of –101 dBc/Hz offset 100 kHz from the carrier. When fabricated on a multiproject wafer using a 0.13-µm semiconductor process from Silterra, the power consumption is a low 8.64 mW because of the low voltage supply.

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